In the Claims:

1. (Currently amended) Method for manufacturing an array of semiconductor devices on a substrate, each device having a floating gate, comprising:

first forming isolation zones in the substrate,

thereafter forming a floating gate separator on the isolation zones at locations where separations between adjacent floating gates are to be formed,

after forming the floating gate separator, forming the floating gates, with spacers adjacent thereto, on the substrate between parts of the floating gate separator, and

thereafter removing the floating gate separator so as to obtain slits in between neighboring floating gates.

2. (Currently amended) ~~Method according to claim 1, furthermore comprising, after forming of the floating gate separator and before forming of the floating gate,~~ Method for manufacturing an array of semiconductor devices on a substrate, each device having a floating gate, comprising:

first forming isolation zones in the substrate,

thereafter forming a floating gate separator on the isolation zones at locations where separations between adjacent floating gates are to be formed,

after forming the floating gate separator, reducing the dimensions of the floating gate separator followed by forming the floating gates on the substrate between parts of the floating gate separator, and

thereafter removing the floating gate separator so as to obtain slits in between neighboring floating gates.

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3. (Previously presented) Method according to claim 2, wherein the dimensions of the floating gate separator are reduced to sub-lithographic dimensions.

4. (Previously presented) Method according to claim 3, wherein the dimensions of the floating gate separator are reduced to between 100 nm and 40 nm.

5. (Previously presented) Method according to claim 2, wherein the dimensions of the floating gate separator are reduced by resist shrink.

6. (Previously presented) Method according to claim 2, wherein the dimensions of the floating gate separator are reduced by trim plasma etching.

7. (Previously presented) Method according to claim 2, wherein the dimensions of the floating gate separator are reduced by an isotropic over-etch of the floating gate separator.

8. (Previously presented) Method according to claim 2, wherein the dimensions of the floating gate separator are reduced by phase-shift lithography.

9. (Previously presented) Method according to claim 2, wherein the floating gate separator comprises nitride material.

10. (Previously presented) Method according to claim 2, wherein the floating gate separator comprises at least two layers of different material.

11. (Previously presented) Method according to claim 2, furthermore comprising forming spacers next to the floating gate separator before forming the floating gates.

12. (Currently amended) An array of semiconductor devices with a floating-gate to control-gate coupling ratio, comprising:

a substrate with a planar surface,

an isolation zone in the substrate in and substantially planar with the planar surface,

at least two floating gates extending on the substrate in a first direction, each floating gate partially overlapping the isolation zone and comprising floating gate material,

a slit between the two floating gates, and

a control gate extending laterally with respect to the planar surface over the floating gates,

wherein at least one of the floating gates is provided with a sharp tip of floating gate material both in the first direction and in a second direction including an angle with the first direction.

13. Cancelled

14. (Previously presented) Array of semiconductor devices according to claim 12, wherein at least one of the floating gates has a flat top surface.

15. (Currently amended) Array of semiconductor devices according to claim [[13]] 12, wherein at least one of the floating gates has a flat top surface and wherein array includes a plurality of memory cells, each cell including a control gate configured and arranged as recited in claim 12.

16. (New) Array of semiconductor devices according to claim 12, and wherein array includes a plurality of memory cells, each cell including a control gate configured and arranged as recited in claim 12.

17. (New) Array of semiconductor devices according to claim 16 wherein each of the memory cells is a nonvolatile memory cell.

18. (New) Method of claim 1, wherein the devices are memory cells accessed with word lines and bit lines, and wherein the floating gate separator is arranged to separate along the direction of the word lines.

19. (New) Method of claim 1, wherein the floating gate separator is not arranged to separate the floating gates in the direction of the bit lines.